

CLAIMS

What is claimed is:

- 1 1. A verification test bench system for testing a system-on-a-chip (SOC) interface of an
2 SOC, said verification test bench system comprising:
3 a verification interface model connected to said SOC interface; and
4 a test bench external bus interface unit (EBIU) connected to said verification interface
5 model,
6 wherein said test bench EBIU is connected to a SOC EBIU within said SOC.
- 1 2. The verification test bench system in claim 1, wherein said SOC EBIU allows a test case
2 running in said SOC to control both said SOC interface and said verification interface model.
- 1 3. The verification test bench system in claim 1, wherein said SOC interface and said
2 verification interface model are programmed by a test case running in said SOC.
- 1 4. The verification test bench in claim 3, wherein said test case utilizes the same software
2 driver to configure and control said SOC interface and said verification interface model.
- 1 5. The verification test bench in claim 3, wherein said test case utilizes different software
2 drivers to configure and control said SOC interface and said verification interface model.

1 6. The verification test bench system in claim 1, wherein said verification interface model
2 tests an operational capability of said SOC interface.

1 7. The verification test bench system in claim 1, further comprising at least one additional
2 verification interface model connected to said test bench EBIU for testing additional types of SOC
3 interfaces.

1 8. A verification test bench system for testing a system-on-a-chip (SOC) interface of an
2 SOC, said verification test bench system comprising:
3 a verification interface model connected to said SOC interface; and
4 a test bench external bus interface unit (EBIU) connected to said verification interface
5 model,
6 wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and
7 wherein said test bench EBIU and said SOC EBIU are mastered by the same processor in
8 said SOC.

1 9. The verification test bench system in claim 8, wherein said SOC EBIU allows a test case
2 running in said SOC to control both said SOC interface and said verification interface model.

1 10. The verification test bench system in claim 8, wherein said SOC interface and said
2 verification interface model are programmed by the same test case running in said SOC.

- 1 11. The verification test bench in claim 10, wherein said test case utilizes the same software
2 driver to configure and control said SOC interface and said verification interface model.
- 1 12. The verification test bench in claim 10, wherein said test case utilizes different software
2 drivers to configure and control said SOC interface and said verification interface model.
- 1 13. The verification test bench system in claim 8, wherein said verification interface model
2 tests an operational capability of said SOC interface.
- 1 14. The verification test bench system in claim 8, further comprising at least one additional
2 verification interface model connected to said test bench EBIU for testing additional types of SOC
3 interfaces.
- 1 15. A verification test bench system for testing a system-on-a-chip (SOC) interface of an
2 SOC, said verification test bench system comprising:
3 a verification interface model connected to said SOC interface; and
4 a test bench external bus interface unit (EBIU) connected to said verification interface
5 model,
6 wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and
7 wherein said test bench EBIU and said SOC EBIU are mastered by the same processor in
8 said SOC, such that said SOC interface and said verification interface model are programmed by
9 the same test case running in said SOC.

- 1 16. The verification test bench system in claim 15, wherein said SOC EBIU allows said test
2 case to control both said SOC interface and said verification interface model.
- 1 17. The verification test bench in claim 15, wherein said test case utilizes the same software
2 driver to configure and control said SOC interface and said verification interface model.
- 1 18. The verification test bench in claim 15, wherein said test case utilizes different software
2 drivers to configure and control said SOC interface and said verification interface model.
- 1 19. The verification test bench system in claim 15, wherein said verification interface model
2 tests an operational capability of said SOC interface.
- 1 20. The verification test bench system in claim 15, further comprising at least one additional
2 verification interface model connected to said test bench EBIU for testing additional types of SOC
3 interfaces.
- 1 21. A method of testing a system-on-a-chip (SOC) interface of an SOC, said method
2 comprising:
3 connecting a verification interface model to said SOC interface;
4 connecting a test bench external bus interface unit (EBIU) to said verification interface
5 model;

6 connecting said test bench EBIU to a SOC EBIU within said SOC; and
7 comparing said SOC interface with said interface model.

1 22. The method in claim 21, further comprising allowing, through said SOC EBIU, a test case
2 running in said SOC to control both said SOC interface and said verification interface model.

1 23. The method in claim 21, further comprising programming said SOC interface and said
2 verification interface model by a test case running in said SOC.

1 24. The method in claim 23, wherein said test case utilizes the same software driver to
2 configure and control said SOC interface and said verification interface model.

1 25. The method in claim 23, wherein said test case utilizes different software drivers to
2 configure and control said SOC interface and said verification interface model.

1 26. The method in claim 21, wherein said comparing process tests an operational capability of
2 said SOC interface.

1 27. The method in claim 21, further comprising:
2 connecting at least one additional verification interface model to said test bench EBIU;
3 and
4 testing additional types of SOC interfaces.

1 28. A program storage device readable by machine tangibly embodying a program of
2 instructions executable by the machine to perform a method for testing a system-on-a-chip (SOC)
3 interface of an SOC, said method comprising:
4 connecting a verification interface model to said SOC interface;
5 connecting a test bench external bus interface unit (EBIU) to said verification interface
6 model;
7 connecting said test bench EBIU to a SOC EBIU within said SOC; and
8 comparing said SOC interface with said interface model.

1 29. The program storage device in claim 28, wherein said method further comprises allowing,
2 through said SOC EBIU, a test case running in said SOC to control both said SOC interface and
3 said verification interface model.

1 30. The program storage device in claim 28, wherein said method further comprises
2 programming said SOC interface and said verification interface model by a test case running in
3 said SOC.

1 31. The program storage device in claim 30, wherein said test case utilizes the same software
2 driver to configure and control said SOC interface and said verification interface model.

1 32. The program storage device in claim 30, wherein said test case utilizes different software
2 drivers to configure and control said SOC interface and said verification interface model.

1 33. The program storage device in claim 28, wherein said comparing process tests an
2 operational capability of said SOC interface.

1 34. The program storage device in claim 28, wherein said method further comprises:
2 connecting at least one additional verification interface model to said test bench EBIU;
3 and
4 testing additional types of SOC interfaces.

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